AN OBJECT-ORIENTED APPROACH FOR THE HIERARCHICAL DESIGN OF VLSI MULTICHIP SYSTEMS[1]

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Executive Summary

Object-oriented approach is applied to develop building blocks (models) of a VLSI multichip system for packaging simulations. In conjunction with hierarchical design, our approach reduces the complexity of modeling and increases reusability of models.

Extended Abstract

Interconnections and packages are among the dominant factors that limit the performance of future integrated circuits. This is especially true for high-speed and high-density electronic systems. Advanced VLSI multichip systems usually contain multilevel interconnections and packages which complicate the analysis and design of the entire system. Although advanced CAD tools have been developed for detailed simulations of such systems in different aspects (electrical or thermal/mechanical, etc.) [1], designers rarely pay much attention to important issues such as design data management and automatic simulation model generation which could increase their productivity. Part of the reason is due to the complexity of design database included in multilevel interconnections and the package of a multichip assembly or module such as decomposition (e.g., chips on a board), taxonomy (e.g., lossy or lossless line, MCM substrate or multilayered printed wire board, etc.), coupling (e.g., drivers, receivers and interconnections in a transmission line system, etc.), and design attributes specifications (e.g., power disspation of each chip or substrate dielectric, etc.).

Fortunately, the hierarchical nature of multilevel interconnections and packages in a VLSI system reduces the complexity of representation scheme in the design process. The use of hierarchy involves dividing a system into subsystems and then repeating this operation on subsystems until the complexity of the subsystems is at a desired abstraction level [2]. This increases the efficiency of computer-aided design processing.

In this paper, an object-oriented approach is applied to represent and develop a design database which encompasses different component models (model base) for multilevel interconnects and packaging structure. The model components are organized in two major libraries termed Chip model library and Package model library. Chip model library includes physical, thermal, and electrical (especially peripheral models such as drivers, receivers, etc.) information of chips with different levels of complexity and abstraction. Package

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model library includes models for different types of boards, modules (or only substrates when multichip modules are considered), and multilevel interconnects (which also include discontinuities such as bends, vias, and crossovers, etc.). Automatic model generation for simulation is done by effective interface and coupling between these two major libraries as shown in Figure 1.

Object–oriented design and object–oriented programming support data abstraction (class and objects), inheritance and modularity [3]. The "generalization–specialization", and "whole–part (or component–subcomponent)" concepts [4] provided in object–oriented design are used to facilitate the implementation of taxonomy, decomposition and coupling for the development of design database (libraries) and automatic model generation for simulation. For example, compared with the pMOS/nMOS model in a lossless transmission line simulator UANTL [5], SPICE model is more specialized (with added details). Accordingly, in our implementation of Chip model library, the SPICE pMOS/nMOS model is just an inherited class from the more general UANTL class with specialized parameters being included. As an illustration for decomposition, consider the implementation of a multistage CMOS inverter in Chip model library. Model designers only have to define a cascaded CMOS inverter class with predefined inverter class as its member object (subcomponent). In this manner, not only the complexity of the development of libraries can be reduced, but the reusability of the software building blocks (models) increased. The building of a transmission line system for circuit simulation is accomplished by retrieving models from Packaging model library and Chip model library and then sending messages to those models (objects) to construct a SPICE like network. This is a typical coupling scheme of model generation for simulations.

Currently the described hierarchical structures of Packaging model library and Chip model library for supporting the VLSI multichip system design are implemented in C++ programming language and reside in an existing CAD framework called Packaging Design Support Environment (PDSE) [6] which integrates several software tools for electronic packaging simulation.

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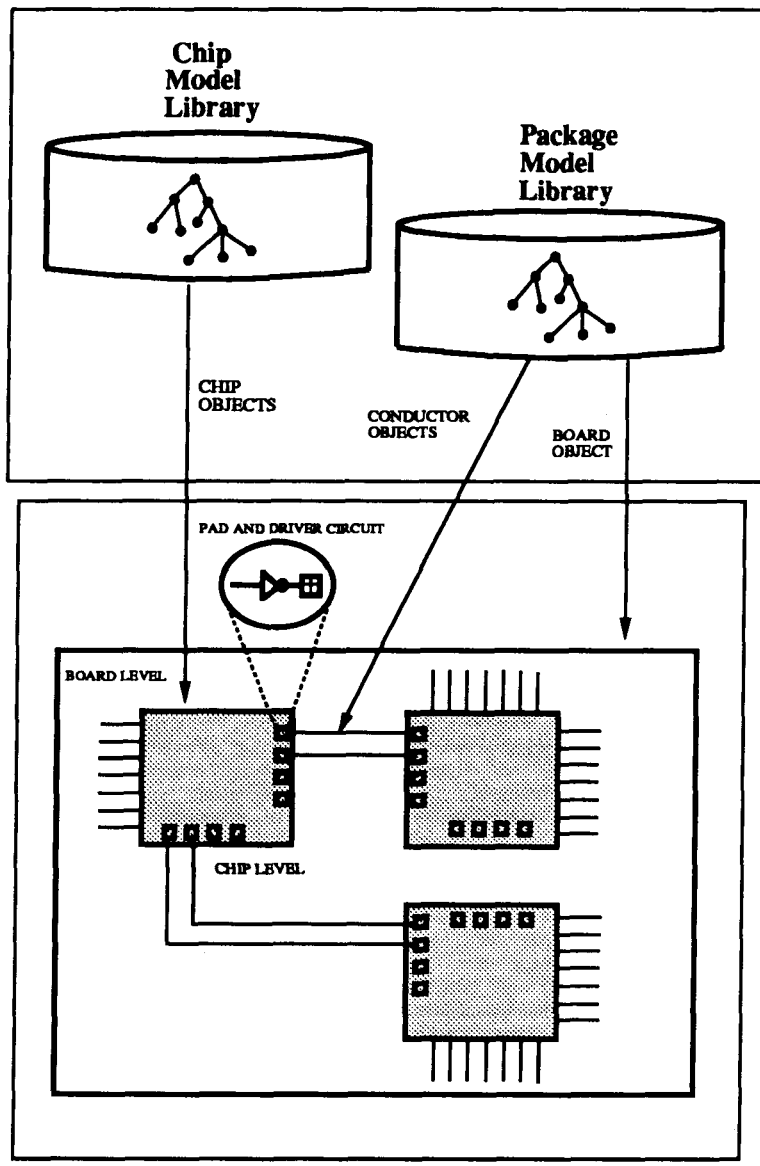

Figure 1: Simulation model generation for the hierarchical design of a VLSI multichip system.